ABSTRACT

A JTAG-programmable IC includes a memory array having redundant columns, a partial-width data register, and a full-width bitline register. A programming bitstream is shifted into the data register in discrete portions, with each portion being loaded into the bitline latch before the next portion is shifted into the data register. The programming bitstream portions fill the bitline latch sequentially unless a count indicator for a particular portion matches a predetermined defective column value, in which case that bitstream portion is rerouted to a region of the bitline latch associated with the redundant columns of the memory array. The count indicator is incremented with each new bitstream portion shifted into the data register. Once the programming bitstream is fully loaded into the bitline latch, the data is programmed into a selected row of the memory array in page mode.